UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,507	09/30/2003	Eric J. Strang	231751US6YA	1662

22850 7590 04/04/2011

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, L.L.P.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

NOTIFICATION DATE	DELIVERY MODE
04/04/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	10/673,507	STRANG, ERIC J.	
	Examiner	Art Unit	
	AKASH SAXENA	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-11,14-44,46-48,51-74 and 78-80* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-11,14-44,46-48,51-74 and 78-80* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/18/09 12/16/2010*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20100905*.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-7,9-11,14-4448,51-74 and 78-80 has/have been presented for examination based on amendment filed on 08/26/2010.
2. Claim(s) 1, 38 and 78 is/are amended.
3. An IDS filed on 12/16/2010 is considered.
4. Correction of inventorship in acknowledged.
5. Claim(s) 1-7,9-11,14-48,51-74 and 78-80 remain rejected under 35 USC § 112.
6. Claims 1-7, 9-11, 14-21, 29-30, 32-34, 37, 79 and 38-44, 46-48, 51-58, 66-67, 69-71, 74, 80 and 78 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sonderman**, in view of **Jain**, further in view of **Tan**.
7. Claims 22 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sonderman**, in view of **Jain**, further in view **Tan**, further in view of I Yunemura.
8. Claims 23-28 and 60-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sonderman**, in view of **Jain**, further in view of **Tan**, further in view of **Chen**.
9. Claims 31, 36, 68 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sonderman**, in view of **Jain**, further in view **Tan**, further in view of N**ikoonahad**.
10. Claims 35 and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sonderman**, in view of **Jain**, further in view **Tan**, further in view of **Fatke**.
11. This action is made Final.

Examiner's Recommendation

12. Applicant's remarks on Pg. 25 last paragraph – Pg.26 first paragraph are noted. If the applicant *claims* the structure of Fig.3 elements 302, 308, 312 and 304 of the how the simulation is distributed among APC and on tool simulators, with reuse features as disclosed in [0047][0048] in remarks, to expedite the simulation in a time-frame shorter than the process time, further compact prosecution may be possible and examiner would consider such an amendment. Examiner would welcome an interview request with proposed amendment in the above line of thought.

Response to Arguments for Rejection under 35 USC 112¶1st

Therefore all rejections under 35 USC 112¶1st are withdrawn **based on the arguments and citation by applicant in view of the support and interpretation below.**

(Argument 1) Applicant has argued in Remarks Pgs.18-22:

> Hence, Applicant discloses 1) a physical model 106 including a spatially resolved model of the physical geometry of the tool 102, 2) physical model 106 implemented in commercially available software such as ANSYS or FLUENT to solve a spatially resolved model, 3) the setting of boundary and internal conditions, 4) repeated running of simulations concurrently with the process, and 5) using physical sensor measurements to repeatedly update boundary conditions of the first principles simulation model.

(Response 1) Applicant's argument in items 1) - 5) are found to persuasive in view of cited paragraphs [0035][0036][0057][0091] and [0092] of the specification which disclose "*setting initial and boundary condition for a spatially resolved model ([0092]) of physical geometry of the semiconductor processing tool*". Further this underlined rejection is withdrawn in view of above.

(Argument 2) Applicant has argued in Remarks Pg.23-26:

> Moreover, "solving the computer-encoded differential equations of the first principles simulation model for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed," is enabled as noted in the previously filed Appeal Brief:
> ...
>
> Hence, the examiner should now understand as before (when the former 112, first paragraph, rejections were removed based on this information) that it is the combination of one or more of the network architecture of FIG. 3, the sharing of model results done for one condition set to other similar or identical tools operating later under the same or similar conditions, the reuse of prior solutions of proven convergence, the reuse of the known solutions as initial conditions for first principles simulation, etc. and **not the details of the model itself [1]** which enable the invention to solve the computer-encoded differential equations of the first principles simulation model for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed.

(Response 2) Essentially applicant has pointed that the limitation "*solving the computer-encoded differential equations of the first principles simulation* ***model for the spatially resolved model*** ***in a time frame shorter in time than the actual process being performed***." Is enabled using the following from the specification [0047]-[0048] states the following:

First, the limitations are now read as being enabled because the results are either stored in the lookup table (similar to historical database) or due to code parallelization (like in distributed code), both of which lead to the execution of s*patially resolved model* ***in a time frame shorter in time than the actual process being performed***. With the interpretation the rejection is withdrawn.

Secondly, applicant has admitted that the spatially resolved model for he first principle simulation are well known in the art **(**See [1] above in applicant's arguments) and **are not the reason** the execution of *spatially resolved model in a*

time frame shorter in time than the actual process being performed. Also shown is the Kee example by applicant.

Response to Arguments for Rejection under 35 USC 103

(Argument 3) Applicant has argued in Remarks Pg.27-29:

> There is no detail here of a spatially resolved model of a physical geometry of the semiconductor processing tool or the setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool.

(Response 3) Examiner has cited Sonderman Col.7 Lines 21-35 which states:

> Turning now to FIG. 5, a flowchart representation of the steps for performing the process simulation function described in block 440 of FIG. 4, is illustrated. The system 100 prepares one or more process models for simulation (block 510). The models that are prepared for simulation may include the device physics model 310, the process model 320, and **the equipment model 330.** The number of models defined by the system 100 generally depends upon the interactions of model-components that are to be examined by the simulator 340. In other words, the system 100 determines which components in a model are to be modified and which components are to be monitored for reactions caused by the original component modification. ...

Here the equipment model is mapped to the spatially resolved model of "the physical geometry of the semiconductor processing tool" as pointed by applicant present in Sonderman Col.5 Lines 62-67. The temperature response & pressure response cannot be ascertained without setting initial and boundary conditions, as indicated by original component models and modifications thereof in the section above. Sonderman Col.6 Lines 64 –Col.7 Line 20 disclose validation of the model, which would not be possible without initializing the models to conditions present in the actual equipment.

As Sonderman states in Col.8 Lines 7-11:

> ...For example, the system 100 invokes a temperature variability of plus or minus 3% of a defined operating temperature into the equipment model 330 to simulate the real online manufacturing effects of temperature variations in an actual processing environment.

Here the 3% represents a type of boundary in equipment model for example.

(Argument 4) Applicant has argued in Remarks Pg.28-29:

> Moreover, statistical models, like Sonderman et al (and Tan et al), do not have initial and boundary conditions, but rather are models which simply correlate inputs and outputs of a process based on statistical data from previous process runs. These models also do not solve for a variable over a gridded spatial domain, but instead use statistics to provide predictions about the end result that would be obtained if a process were run in a certain manner....

(Response 4) Applicant appears to alleging that Sonderman's models are statistical models because they use fed back data from previous computations. Applicant is reminded of their own statements and citations from the specification where they have stated that the inventive concept of their invention is the ability to use data from previous computations stored in libraries. How applicant has come to conclusion that no initial and boundary conditions are specified in Sonderman's models from this statistical models allegation is unclear.

(Argument 5) Applicant has argued in Remarks Pg.30:

> With regard to the first emphasized section above, that section states that "the process control environment 180 can receive data from the manufacturing environment 170," there is no indication that the received data is data for setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool. The received data may well have been metrology data, which would have been data taken on a sample sent to the metrology tool 150.

(Response 5) In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., The received data may well have been metrology data, which would have been data taken on a sample sent to the metrology tool 150) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The claim requires " setting initial and boundary conditions for a spatially resolved model of a physical geometry of the

semiconductor processing tool based on said process data related to the actual process being performed by the semiconductor processing tool;". There is no requirement that received data does not have to metrology data and Sonderman does not state that it is metrology data in the Col.7 Lines 8-20. Even if the metrology data is used in the simulation that does not change the fact the boundary conditions (e.g. variations in temperature as taught in Sonderman Col.8 Lines 7-11) are not set for the equipment model.

(Argument 6) Applicant has argued in Remarks Pg.31:

> Secondly, the combination of Sonderman et al and Jain et al is improper because it is without a reasonable expectation of success and a person skilled in the art at the time of the invention would not have been motivated to risk control of a semiconductor processing unit to the unproven technology of Jain et al's MPE.

(Response 6) In response to applicant's argument that a person skilled in the art at the time of the invention would not have been motivated to risk control of a semiconductor processing unit to the unproven technology of Jain et al's MPE, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Specifically, whether an art is predictable or whether the proposed modification or combination of the prior art has a reasonable expectation of success is determined at the time the invention was made. In re Rinehart (Citation omitted). In this case even is the

Jain makes real time solving possible by providing *model-solving capacity in real time when differential equations are present in the model* (like thermal patterns in semiconductor wafer model) (Jain: Abstract) which Sonderman discloses *as differential equations*, being present and being solved for (Sonderman: Col.8 Lines 1-43). Since Sonderman and Jain are in the same field of endeavor, which is to solve differential equations related to semiconductor processing there is reasonable expectation of successes.

MPEP also states:

> I. < OBVIOUSNESS REQUIRES ONLY A REASONABLE EXPECTATION OF SUCCESS
> The prior art can be modified or combined to reject claims as prima facie obvious as long as there is a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986) (Claims directed to a method of treating depression with amitriptyline (or nontoxic salts thereof) were rejected as prima facie obvious over prior art disclosures that amitriptyline is a compound known to possess psychotropic properties and that imipramine is a structurally similar psychotropic compound known to possess antidepressive properties, in view of prior art suggesting the aforementioned compounds would be expected to have similar activity because the structural difference between the compounds involves a known bioisosteric replacement and because a research paper comparing the pharmacological properties of these two compounds suggested clinical testing of amitriptyline as an antidepressant. The court sustained the rejection, finding that the teachings of the prior art provide a sufficient basis for a reasonable expectation of success.); Ex parte Blanc, 13 USPQ2d 1383 (Bd. Pat. App. & Inter. 1989) (Claims were directed to a process of sterilizing a polyolefinic composition with high-energy radiation in the presence of a phenolic polyester antioxidant to inhibit discoloration or degradation of the polyolefin. Appellant argued that it is unpredictable whether a particular antioxidant will solve the problem of discoloration or degradation. However, the Board found that because the prior art taught that appellant's preferred antioxidant is very efficient and provides better results compared with other prior art antioxidants, there would have been a reasonable expectation of success.).
> >II. < AT LEAST SOME DEGREE OF PREDICTABILITY IS REQUIRED; APPLICANTS MAY PRESENT EVIDENCE SHOWING THERE WAS NO REASONABLE EXPECTATION OF SUCCESS
> **Obviousness does not require absolute predictability, however, at least some degree of predictability is required. Evidence showing there was no reasonable expectation of success may support a conclusion of nonobviousness. In re Rinehart, 531 F.2d 1048,** 189 USPQ 143 (CCPA 1976) ...
> ...The court reversed, finding there was no reasonable expectation that a process combining the prior art steps could be successfully scaled up in view of unchallenged evidence showing that the prior art processes individually could not be commercially scaled up successfully.). See also Amgen, Inc. v. Chugai Pharmaceutical Co., 927 F.2d 1200, 1207-08, 18 USPQ2d 1016, 1022-23 (Fed. Cir.), cert. denied,502 U.S. 856 (1991) (In the context of a biotechnology case, testimony supported the conclusion that the references did not show that there was a reasonable expectation of success.); In re O 'Farrell, 853 F.2d 894, 903, 7 USPQ2d 1673, 1681 (Fed. Cir.

1988) (The court held the claimed method would have been obvious over the prior art relied upon because one reference contained a detailed enabling methodology, a suggestion to modify the prior art to produce the claimed invention, and evidence suggesting the modification would be successful.).
III. >< PREDICTABILITY IS DETERMINED AT THE TIME THE INVENTION WAS MADE
Whether an art is predictable or whether the proposed modification or combination of the prior art has a reasonable expectation of success is determined at the time the invention was made. Ex parte Erlich, 3 USPQ2d 1011 (Bd. Pat. App. & Inter. 1986) (Although an earlier case reversed a rejection because of unpredictability in the field of monoclonal antibodies, the court found "in this case at the time this invention was made, one of ordinary skill in the art would have been motivated to produce monoclonal antibodies specific for human fibroplast interferon using the method of [the prior art] with a reasonable expectation of success." 3 USPQ2d at 1016 (emphasis in original).). 2143.03 [R-6] All Claim Limitations Must Be **>Considered< **"All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

In this case Jain (1994) was well known at the time of invention (2003). As **Moore's law** states that processing technology/speed/integrated circuit doubles approximately every 2-3 years, therefore the disclosure in Jain would not have been so futuristic. (w.r.t. Ex Parte Erlich above). Further applicant has not provided any evidence that there is **no reasonable expectation of success may support a conclusion of nonobviousness. In re Rinehart (as noted in MPEP above).** the Applicant has merely alleged that one would not be motivated to combine whereas the teaching of Jain clearly point to direct application in the field of the Sonderman.

(Argument 7) Applicant has argued in Remarks Pg.33-34:

> Thirdly, Tan et al do not teach solving the computer-encoded differential equations of the first principles simulation model for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed.
>
> The examiner relied on Tan et al for their teaching of at col. 2, lines 7-10, of model- based real time process control using in situ inputs, process models, and process control strategies to correctly process control parameters during the process run. Yet, a "model- based" real time process control does not specify when the model is completed, only that the "process control" in Tan is real time and does not indicate that a solution to computer- encoded differential equations of the first principles simulation model for a spatially resolved model of a physical geometry of the semiconductor processing tool can be obtained in a time frame shorter in time than the actual process being performed.

(Response 7) First, Tan is only used to clarify that what is now implicit in the Sonderman's teachings. Applicant has admitted on Remarks Pg.25-26 first paragraph:

> the sharing of model results done for one condition set to other similar or identical tools operating later under the same or similar conditions, the **reuse of prior solutions of proven convergence**, the **reuse of the known solutions as initial conditions for first principles simulation**, etc. and **not the details of the model itself [1]** which enable the invention to solve the computer-encoded differential equations of the first principles simulation model for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed.

Reuse of the prior solutions as one used in Sonderman as fed back data is used to expedite the model processing. Examiner has stated in the rejection as well that Arguendo, even if **Sonderman and Jain** do no explicitly teach said first principles simulation result being produced in a time frame shorter in time than the actual process being performed **Tan** teach the above limitation. .

(Argument 8) Applicant has argued in Remarks Pg.36-39:

> Moreover, the previously filed declaration noted above attested to the fact that neither Sonderman et al nor Tan et al use a first principles simulation model. Rather, as attested to, the models in these references are 1) simplified models based on former approximate solutions or 2) statistical or "learned" models tracking how the systems are expected to behave. Thus, even if the reading of the whole of Tan et al is discredited by the examiner, then the claim's recitation of solving computer-encoded differential equations of the first principles simulation model for a spatially resolved model of a physical geometry of the semiconductor processing tool is still no_._tt met because Tan et al do not use a first principles simulation model. In fact, as noted above, only Applicants have realized that computer- encoded differential equations of the first principles simulation model for a spatially resolved model of a physical geometry of the semiconductor processing tool can be solved in a time frame shorter in time than the actual process being performed.

(Response 8) In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231

USPQ 375 (Fed. Cir. 1986). Sonderman & Jain is used to show the teaching of models setting boundary conditions, with use of "feed-back data", details of such feedback and feed-forward are shown in Tan which also states that such execution is done in time frame shorter than actual processing.

Consideration and comments on applicant's ***rebuttal evidence*** are addressed below:

US Patent 6185472: This shows shorted simulation time (2hrs) which still exceeds applicant's alleged process time. First applicant did not claim all simulations are and can be completed in time frame shorter and to the contrary state they cannot be (Specification: [0035][0037]). Further even if true in this case Tan teaches that simulations are completed before actual process completes to provide input to the actual process. So unless applicant is presenting evidence contrary to and invalidating the teachings of US Patent 6263255 by Tan et al, the argument is unpersuasive.

US Patent 7047095: No reference appears to be made to a model, hence is not persuasive.

US Patent 6587744: Examiner disagrees that this reference states "feedback and feed forward process control where the result of a simulation would not be obtained during the performance of the actual process to control the actual process being performed, and therefore would not be used to control the actual process performed by the semiconductor processing tool". On the contrary the cited section states:

> Feed-forward control algorithms may, in certain embodiments, be used to adjust process targets for closed loop feedback control. The supervising station may have a user interface by which different feedback or feed-forward model formats (single or multi-variate) may be interactively

> selected based upon experimental or predicted behavior of the system, and may also permit users to utilize their own models for run-to-run control.

This implies that the models are used to adjust the process target using feed forward models and therefore models must finish execution to affect that adjustment of process target. This reference appears to buttresses examiner position as well.

(Argument 9) Applicant has argued in Remarks Pg.39-40:

> Fourthly, in support of Applicants' position on the non-obviousness of the claims, the previously filed declaration attested to the fact that, prior to the filing of this application, a two-dimensional axisymmetric time-evolution temperature simulation of a chuck with a wafer, a plasma heat load, and a coolant heat removal was performed. By setting initial and boundary conditions to values appropriate for the physical chuck setup, a time-evolving solution was obtained in less than 5 seconds, for a process of nominal duration of 60 seconds…

(Response 9) In assessing the probative value of an expert opinion, the examiner must consider the nature of the matter sought to be established, the strength of any opposing evidence, the interest of the expert in the outcome of the case, and the presence or absence of factual support for the expert's opinion. (MPEP 716.01(c) III). In this case, the inventor is acting as expert. Further the unexpected results appear to be due to reuse of known solutions as presented in Sonderman therefore are not unexpected.

(Argument 10) Applicant has argued in Remarks Pg.40-42:

> Yet, the fitting functions in Chen (as seen from Figures 3a and 3b) are applied to adjust (i.e., fit) the simulated result to the actual result. The fitting functions are not applied to set initial conditions for cells in the first principles simulation, as claimed. Rather, the fitting functions are applied to a generated simulation result to make the simulation result already calculated agree with the observed data.
> …
> Thus, a combination of Chen with Sonderman et al and Jain et al and Tan et al would not yield these claim features.

(Response 10) The calibration stage is the where the input and outputs are fitted (fitting function) to match the real output. The calibration stage is initial condition

inputting stage, before the simulation data is provided for actual run to the model as well as the tool. It unclear how initial conditions are not fitted to produce the expected result and more needs to be added to the claim what initial condition mean. Examiner finds applicant's arguments unpersuasive. Further, In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

---- This page left blank after this line. ----

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claims 1-7, 9-11, 14-21, 29-30, 32-34, 37, 79 and 38-44, 46-48, 51-58, 66-67, 69-71, 74, 80 and 78 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter) further in view U.S. Patent No. 6,263,255 issued to Tan et al (Tan hereafter).

Regarding Claim 1 (updated 3/2/11)

Sonderman teaches a method to controlling a process performed by a semiconductor-processing tool (**Sonderman**: Summary, at least in Col.2 Lines 10-17; Col.3 Lines 45-49) by ***inputting*** *a inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool* (**Sonderman**: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model.

Further, **Sonderman** teaches ***inputting*** *process data relating to an actual process being performed by the semiconductor-processing tool* (**Sonderman**: at least in Col.3 Lines 50-67; *Col.7 Lines 8-20*).

Further, **Sonderman** teaches *setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool* (**Sonderman**: Col.7 Lines 21-35; Col.6 Lines 64 –Col.7 Line 20; Col.8 Lines ; Col.8 Lines 7-11) where the equipment model is the spatially resolved model and initial

conditions are set for model validation (Col.6 Lines 64 –Col.7 Line 20) ready for modification (Col.7 Lines 21-35) and boundary conditions as exemplified as temperature variations of 3% (Col.8 Lines 7-11). Sonderman teaches *the above based on said process data related to the actual process being performed by the semiconductor processing tool* (**Sonderman**: Col.7 Lines 7-20).

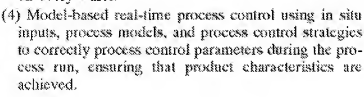
Sonderman does not teach first principle model including a set of computer encoded differential equations.

Jain teaches ***solving*** *the computer-encoded differential equations of the first principles simulation model* using MPE engine, which can be applied to wafer processing (**Jain**: Abstract; Pg. 372 Section V Dedicated MPE).

Further, **Sonderman & Jain teaches *providing*** *a first principles simulation result process* (**Sonderman**: Fig. 1-3 *Col.7 Lines 4-7; Col.3 Lines 56-63*) *from the solution of the computer- encoded differential equations* (**Jain**: Abstract & Pg. 372 Section V Dedicated MPE) *solved concurrently with the actual process being performed* (**Sonderman**: at least in *Col.9 Lines 40-52;* Col.3 Lines 50-67; Col.7 Lines 8-20) *and **using** the first principles simulation result obtained during the performance of the actual process to control the actual process performed by the semiconductor processing tool* (**Sonderman**: at least in Col.4 Lines 48-64; Fig.1-8; Col.2 Lines 10-17).

Arguendo, even if **Sonderman and Jain** do no explicitly teach said first principles simulation result being produced in a time frame shorter in time than the actual process being performed **Tan** teach the above limitation.

Tan *teaches said first principles simulation result being produced in a time frame shorter in time than the actual process being performed as in Col.2 Lines 7-12 as:*



(4) Model-based real-time process control using in situ inputs, process models, and process control strategies to correctly process control parameters during the process run, ensuring that product characteristics are achieved.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Jain** to **Sonderman** to solve differential equation for the semiconductor processing tool. **Sonderman** teaches building various models, which work in real-time feedback control simulating actual semiconductor modeling process (**Sonderman**: Fig.1; Col.7 Lines 8-20), while **Jain** makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (**Jain**: Abstract).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of ***Tan*** *to* ***Sonderman*** *to facilitate the simulation as defined in Fig.2. The motivation to combine is that both* ***Tan*** *and* ***Sonderman*** *teach performing simulation of semiconductor assembly line including the tools and the processes running on them (****Tan****: Col.5 Line 63-Col.6 Line 8;* ***Sonderman****:* ***Sonderman****: Col.7 Lines 4-7; Col.3 Lines 56-63, Fig.1-3).*

Regarding Claim 38 (updated 3/2/11)

System claim 38 (**Sonderman**: Fig.1, **Tan**: 6-7) discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 78 (updated 3/2/11)

Apparatus claim 78 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 2

Sonderman teaches directly inputting the *process* data relating to the *actual* process *being* performed by the semiconductor-processing tool from at least one of physical sensor (e.g. Scatterometry data, overlay data, dimensional data) and a metrology tool physically mounted on the semiconductor-processing tool (**Sonderman**: at least in Col.4 Lines 31-48; Col.4-8; Fig.1, 7; *Col.7 Lines 8-20*).

Regarding Claims 3-5

Sonderman teaches indirectly inputting the *process* data relating to the *actual* process performed by the semiconductor-processing tool from one of the manual input devices and a database as manual fashion data retrieval and automatic data retrieval; inputting data recorded from the previous run; inputting the data set by a simulation operator (**Sonderman**: at least in Fig.1-3 Col.1; Col.4-7; Col.7 Lines 8-20).

Regarding Claims 6-7, 9

Sonderman teaches inputting process data relating to at least one of the physical characteristics of the semiconductor-processing tool and semiconductor tool environment, data relating to at east on of the characteristics and a result of a process performed by the semiconductor processing tool; inputting fundamental equations necessary to perform first principle simulation for the desired simulation

result (**Sonderman**: at least in Col.5 Lines 10-18; Col.6 Lines 48-63; Col.9 (equations); Col.5-9; Fig 1-3; Col.7 Lines 8-20). **Sonderman** and **Jain** teach inputting fundamental equations as the set of computer encoded differential equations (**Sonderman**: Col.9 (equations); **Jain**: Pg. 372 Section V Dedicated MPE, Abstract).

Regarding Claim 10

Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (**Sonderman**: Fig.2; Col.4 Lines 48-63).

Regarding Claims 11

Sonderman teaches performing first principle simulation independent of the process performed by the semiconductor-processing tool (**Sonderman**: at least in Col.5-8; Fig.3-6 especially col.7).

Regarding Claim 14

Sonderman teaches using the first principles simulation result comprises using the first principles simulation result to perform at least one of detecting, and classifying a fault in the process performed by the semiconductor-processing tool (**Sonderman**: at least in Col.5 Line 56 – Col.6 Line 24).

Regarding Claims 15-19

Sonderman teaches using a network of interconnected resources inside the semiconductor manufacturing facility (**Sonderman**: Semiconductor tools on the factory floor – Col.9 Lines 60-65) to perform first principle simulation (**Jain**: Section

III); using code parallelization among interconnected computational resources to share the computational load of the first principle simulation; sharing simulation information among the interconnected resources to facilitate a process by the semiconductor-processing tool; sharing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principle simulation by different resources; sharing information comprising model changes among the interconnected resources to reduce the redundant refinements of first simulation by different resources (**Sonderman**: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8).

Regarding Claims 20-21

Sonderman teaches remote access to computational and storage resources (**Sonderman**: Col.9 Line 58-Col.10 Line 31) where in wide area network is art inherent.

Regarding Claim 29

Sonderman teaches performing a principle components analysis to determine a relationship between spatial components of said first principles simulation result for the semiconductor processing tool and a set of at least one control variable, said relationship utilized to determine a correction to said set of at least one control variable in order to affect a reduction in the magnitude of said spatial components (**Sonderman**: Col.5 Line 56 – Col.6 Line 23).

Regarding Claim 30

Sonderman teaches first principle simulation controlling at least one of a material processing system, an etch system, a photo resist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (**Sonderman**: at least in Col 4 Lines 18-31; Col.3 Lines 45-49).

Regarding Claim 32

Sonderman teaches inputting various parameters *as tool data* relating to etching, deposition etc. (**Sonderman**: at least in Col.5 Lines 56-67).

Regarding Claim 33

Sonderman teaches inputting physical geometric data as parameters for the equipment model where the equipment could be at least one of a material processing system, an etch system, a photo resist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (**Sonderman**: Col.5 Lines 56-67).

Regarding Claim 34

Sonderman teaches first principles simulation result controlling the semiconductor processing tool by using model output to adjust said process performed by the semiconductor processing tool (**Sonderman**: Col.4 Lines 48-64; Fig.1-2).

Regarding Claim 37

Sonderman teaches inspecting process results and providing input to the first principles simulation for calibration purposes (**Sonderman**: Col.6 Lines 14-24).

Regarding Claim 39

System claim 39 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claims 40-42

System claims 40-42 disclose similar limitations as claims 3-5 and are rejected for the same reasons as claims 3-5 respectively.

Regarding Claims 43-44, 46

System claims 43-46 disclose similar limitations as claims 6-9 and are rejected for the same reasons as claims 6-9 respectively.

Regarding Claim 47

System claim 47 discloses similar limitations as claim 10 and is rejected for the same reasons as claim 10.

Regarding Claim 48

System claims 48 disclose similar limitations as claim 11 and are rejected for the same reasons as claim 11 respectively.

Regarding Claim 51

System claim 51 discloses similar limitations as claim 14 and is rejected for the same reasons as claim 14.

Regarding Claims 52-56

System claims 52-56 disclose similar limitations as claims 15-19 and are rejected for the same reasons as claims 15-19 respectively.

Regarding Claims 57-58

System claims 57-58 disclose similar limitations as claims 20–21 and are rejected for the same reasons as claims 20-21 respectively. *Change in dependency from claim 52 to claim 38 of claim 57 is noted.*

Regarding Claim 66

System claim 66 discloses similar limitations as claim 29 and is rejected for the same reasons as claim 29.

Regarding Claim 67

System claim 67 discloses similar limitations as claim 30 and is rejected for the same reasons as claim 30.

Regarding Claim 69

System claim 69 discloses similar limitations as claim 32 and is rejected for the same reasons as claim 32.

Regarding Claim 70

System claim 70 discloses similar limitations as claim 33 and is rejected for the same reasons as claim 33.

Regarding Claim 71

System claim 71 discloses similar limitations as claim 34 and is rejected for the same reasons as claim 34.

Regarding Claim 74

System claim 74 discloses similar limitations as claim 37 and is rejected for the same reasons as claim 37.

Regarding Claims 79-80

Jain *teaches use of Navier Stokes and other known simulation solutions for solving various simulation problems as initial condition (**Jain**: Pg. 367-368 Section "Governing Rationale" Sub-Section A. Governing Equations).* ***Sonderman*** *also teaches initializing the models with input data (**Sonderman**: Col.7 Lines 8-20).*

14. Claims 22 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Jain, further in view Tan, further in view of IEEE article "Heat Analysis on Insulated Metal Substrates" by Naomi Yunemura et al (Yunemura hereafter).

Regarding Claim 22

Teachings of **Sonderman** and **Jain** are disclosed in claim 1 rejection above. **Sonderman** also teaches that the first principle simulation models the equipment conditions, thereby modeling temperature response and pressure response during various processes (**Sonderman**: at least in Col.5 Lines 62-67). **Jain** also teaches distributed and dedicated hardware implementation to solving wafer problem using computer implemented differential equations (**Jain**: Section III & IV). **Sonderman**, **Jain** & **Tan** do not teach explicitly that such temperature and pressure modeling is done using ANSYS computer code.

Yunemura teaches that heat simulation modeling can be performed using ANSYS computer code (Yunemura: Pg. 1407 Section 1) on a silicon chip.

Motivation to combine **Jain** with **Sonderman** is disclosed above.

*It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Tan** to **Sonderman** to*

facilitate the simulation as defined in Fig.2. The motivation to combine is that both ***Tan*** *and* ***Sonderman*** *teach performing simulation of semiconductor assembly line including the tools and the processes running on them (****Tan****: Col.5 Line 63-Col.6 Line 8;* ***Sonderman****:* ***Sonderman****: Col.7 Lines 4-7; Col.3 Lines 56-63, Fig.1-3).*

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Yunemura to **Sonderman** and **Jain** to create a equipment model as disclosed by **Sonderman**. The motivation to combine would have been that Yunemura teaches heat modeling on a silicon chip affecting the thermal conductivity (Yunemura: Pg.1407 Section 2) based on various thicknesses and **Sonderman** is solving the same issue for the equipment model that for example model the equipment for depositing the various layers and affects on heat and pressure. Further, ANSYS is known in art to be used as thermal & pressure modeling tool based on finite element analysis. Motivation to combine **Jain** and Yunemura is that **Jain** as taught above indicates distributed solving of computer implemented differential equations which Yunemura solves by ANSYS modeling, thereby facilitating in implementation of **Jain**'s teachings.

Regarding Claim 59

System claim 59 discloses similar limitations as claim 22 and is rejected for the same reasons as claim 22.

---- This page left blank after this line. ----

15. Claims 23-28 and 60-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Jain, further in view of Tan, further in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter).

Regarding Claims 23-25

Teachings of **Sonderman**, **Jain** & **Tan** are disclosed in claim 1 rejection above.

Sonderman, **Jain** & **Tan** does not explicitly teach close fitting the solution of the first principle simulation run to thereby set the initial conditions for cells in the first principle simulation; selecting close fitting solutions from a library based on convergence.

Chen teaches close fitting the solution of the first principle simulation run to thereby set the initial conditions for cells in the first principle simulation (**Chen**: Col.6 Lines 26-38); selecting close fitting solutions from a library based on convergence (**Chen**: at least in Col.5 Lines 38 – Col.6 Line 25; Fig 3A-B, Fig.2; Col.4 Line 55 – Col.6 Line 19).

Motivation to combine **Jain** with **Sonderman** is disclosed above.

*It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Tan** to **Sonderman** to facilitate the simulation as defined in Fig.2. The motivation to combine is that both **Tan** and **Sonderman** teach performing simulation of semiconductor assembly line including the tools and the processes running on them (**Tan**: Col.5 Line 63-Col.6 Line 8; **Sonderman**: **Sonderman**: Col.7 Lines 4-7; Col.3 Lines 56-63, Fig.1-3).*

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Chen** to **Sonderman** and **Jain**. The motivation to combine would have been that **Chen** and **Sonderman** both are analogous art concerned with simulating the semiconductor fabrication process and providing the best control parameters to the actual semiconductor-processing tool (**Chen**: at least in Col.3 Lines 19-23).

Regarding Claim 26

Chen teaches that the close-fitting solution library existing on a network of computers connected to semiconductor-processing tool (**Chen**: Fig.2; Col.4 Line 55 –Col.6 Line 19).

Regarding Claims 27-28

Chen teaches calculating solution to the first principle simulation by choosing a coarse grid for solution to the first principle simulation (**Chen**: at least in Col.6 Line 44-Col.7 Line 14) as user defined parameters; further, subsequent solutions by setting the initial conditions to fine grid are made though Gaussian distribution and actual inline data (**Chen**: at least in Col.6 Line 46-51).

Regarding Claims 60-62

System claims 60-62 disclose similar limitations as claims 23-35 and are rejected for the same reasons as claims 23-25 respectively.

Regarding Claim 63

System claim 63 discloses similar limitations as claim 26 and is rejected for the same reasons as claim 26.

Regarding Claims 64-65

System claims 64-65 disclose similar limitations as claims 27-28 and are rejected for the same reasons as claims 27-28 respectively.

16. Claims 31, 36, 68 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Jain, further in view Tan, further in view of U.S. Patent No. 6,812,045 issued to Mehrdad Nikoonahad (Nikoonahad hereafter).

Regarding Claim 31

Teachings of **Sonderman**, **Jain** & **Tan** are disclosed in claim 1 rejection above. **Sonderman** provides examples of the processing tool as etch and photolithography tools (Col.4 Lines 26-31) but **Sonderman**, **Jain** & **Tan** do not explicitly disclose chemical vapor and physical vapor deposition system.

Nikoonahad teaches deposition tools to include chemical vapor and physical vapor deposition system (**Nikoonahad**: Col.24 Lines 3-49).

Motivation to combine **Jain** with **Sonderman** is disclosed above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Nikoonahad** to **Sonderman** and **Jain**. The motivation to combine would have been that **Nikoonahad** and **Sonderman** are analogous art and both are modeling the semiconductor processing and providing feedback to the semiconductor processing tool (**Sonderman**: Abstract; **Nikoonahad**: Col.3; Col.93 Lines 20-35).

Regarding Claim 36

Nikoonahad teaches plurality of computing (as processor)/ storage (as memory) devices connected over network to exchange information between a plurality of computing/storage devices including at least one of model solver parameters, solution status to the first principles simulation, model solutions to the first principles simulation, and solution convergence history for said model solutions (**Nikoonahad**: Col.3 Lines 15-44; Col.68, Lines 41-59).

Regarding Claim 68

System claim 68 discloses similar limitations as claim 31 and is rejected for the same reasons as claim 31.

Regarding Claim 73

System claim 73 discloses similar limitations as claim 36 and is rejected for the same reasons as claim 36.

17. Claims 35 and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Jain, further in view Tan, further in view of U.S. Application 10/472,436 filed by David Fatke et al. (Fatke hereafter).

Regarding Claim 35

Teachings of **Sonderman**, **Jain** & **Tan** are disclosed in claim 1 rejection above.

Sonderman, **Jain** & **Tan** do not teach step of controlling by utilizing at least on of non-linear optimization and multivariate analysis to derive the control model for the process control.

Fatke teaches utilizing at least on of non-linear optimization and multivariate analysis to derive the control model for the process control (**Fatke**: [0011][0012][0035][0050]-[0058][0021]). **Fatke** uses the partial least square (PLS) model to perform multivariate analysis ([0050] to derive the control model for the process control and provide output to the semiconductor-processing tool ([0021]). Further, **Fatke** teaches that the nonlinear optimization is known in the art for creating such models ([0012]).

Motivation to combine **Jain** with **Sonderman** is disclosed above in claim 1.

Motivation to combine **Tan** with **Sonderman** is disclosed above in claim 1.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Fatke** to **Sonderman** and **Jain**. The motivation to combine would have been that **Fatke** and **Sonderman** are analogous art and **Fatke** creates a model form the determining the endpoint of the etching in an etch reactor (**Fatke**: Abstract/Summary), thereby creating a equipment model and the process model for etching, which can be applied to **Sonderman**.

Regarding Claim 72

System claim 72 discloses similar limitations as claim 35 and is rejected for the same reasons as claim 35. Motivation to combine **Jain** with **Sonderman** is disclosed above in claim 38. Motivation to combine **Tan** with **Sonderman** is disclosed above in claim 38.

---- *This page left blank after this line.* ----

Conclusion

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571)272-8351. The examiner can normally be reached on 8:00- 6:00 PM Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kamini S Shah/
Supervisory Patent Examiner, Art Unit 2128

/A. S./
Examiner, Art Unit 2128
Wednesday, March 02, 2011

/David Silver/
Primary Examiner, Art Unit 2128